IN THE CLAIMS

Kindly amend claim 10 as shown in the following claim listing:

1. (original) A method of manufacturing a trench gate semiconductor device comprising the steps of:

providing a silicon device body having a first major surface, the silicon device body having a drain region of a first conductivity type and a body region over the drain region;

forming a trench extending downwards into the silicon device body from the first major surface, the trench having sidewalls and a base;

depositing a nitride liner within the trench to protect the sidewalls;

forming a polysilicon plug at the base of the trench;

thermally oxidising the device to oxidise the polysilicon at the bottom of the trench to form an oxide plug at the base of the trench; and

depositing conductive material within the trench to form a gate.

2. (original) A method according to claim 1 wherein the step of forming a polysilicon plug at the base of the trench forms a doped polysilicon plug at the base of the trench.

3. (original) A method according to claim 2 wherein the step of depositing a doped polysilicon plug at the base of the trench includes depositing polysilicon over the first major surface including the trench and then etching back the doped polysilicon to remove the doped polysilicon from the first major surface leaving the polysilicon at the base of the trench.

4. (original) A method according to claim 2 wherein the step of depositing doped polysilicon includes depositing undoped polysilicon and then carrying out a diffusion process to dope the undoped polysilicon.

5. (previously presented) A method according to claim 1 further comprising the steps of:

thermally oxidising the side wall of the trench to form an oxide layer before depositing the nitride liner over the oxide layer;

etching away the nitride liner and the oxide layer after oxidising the doped polysilicon; and

thermally oxidising the sidewalls to form a thermal oxide gate insulator before depositing conductive material within the trench to form a gate.

6. (previously presented) A method according to claim 1 wherein the step of forming the trench includes providing a mask on the first major surface defining an opening and etching through the opening a trench extending downwards from the first major surface.

7. (original) A method according to claim 6 wherein the mask is an oxide hard mask.

8. (previously presented) A method according to claim 1 wherein the step of depositing conductive material to form a gate includes filling the trench with polysilicon to form a gate.

9. (previously presented) A method according to claim 1 further comprising forming a source implant of first conductivity type at the first major surface adjacent to the trench and forming source, gate and drain electrodes attached to the source implant, the gate and the drain region respectively to complete the trench gate semiconductor device.

10. (currently amended) A trench MOSFET comprising:

a drain region of first conductivity type;

a body region over the drain region;

a trench extending from a first major surface through the body region;

source regions laterally adjacent to the trench at the first major surface;

thermal gate oxide on the side walls of the trench;

a gate electrode in the trench insulated from the body region by the gate oxide;

characterised by a thick oxide plug formed only of thermally oxidised doped polysilicon at the base of the trench extending into the drain region.